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Improving the Performance of Concatenated Convolutional Codes in the Error Floor Region

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Abstract– **The idea of the Bit-Interleaved Coded Modulation with Iterative Decoding (BICM-ID) is applied to classic schemes of both parallel and serial concatenation of convolutional codes (PCCC and SCCC) with Binary Phase Shift Keying (BPSK) modulation. Simulation results show that slightly modified PCCC and SCCC schemes provide significant improved performance of the encoder in the error floor region in terms of much lower bit error rate (BER).**

Keywords– **Turbo codes, serial concatenated convolutional codes, BICM-ID.**

1 Introduction

In 1993 a new class of concatenated codes called turbo codes was introduced [1]. Turbo codes outperform the most powerful codes known to date, but more importantly, they are much simpler to decode. A turbo encoder is a combination of two simple systematic recursive convolutional (RSC) encoders ENCODER1 and ENCODER2, each using a small number of states, as shown in Figure 1. For a block of k information bits, each constituent code generates a set of parity bits. The turbo code consists of the information bits $\boldsymbol{s}$ and both sets of parity, say $\boldsymbol{p_1}$ and $\boldsymbol{p_2}$. The key innovation is an interleaver INT which permutes the original information bits before encoding the second code. If the interleaver is well chosen, the resulting code achieves performance similar to that of Shannon's random codes [2].

Turbo decoding uses two *simple* soft-input soft-output (SISO) decoders, namely DECODER1 and DECODER2, individually matched to the simple constituent codes. Each decoder sends likelihood estimates of the decoded bits to the other decoder, and uses the corresponding estimates from the other decoder as a priori likelihoods. The constituent decoders use the maximum a posteriori (MAP) bitwise decoding algorithm. The turbo decoder iterates between the outputs of the two decoders until reaching satisfactory convergence. The final output is a hard-quantized version of the likelihood estimates of either of the decoders.

The original turbo codes were based on parallel concatenations of convolutional codes (PCCC). Later, similar codes were developed at JPL based on serial concatenation [3] and hence called serially concatenated convolutional code (SCCC). For a block of information bits, the outer encoder generates a codeword whose bits are permuted by an interleaver, and the permuted bits are input to the inner encoder. The output bits of the inner encoder form the codewords of the SCCC, as shown in Figure 2. Serially concatenated codes offer the potential of somewhat better performance than parallel concatenated codes, including lower error floors. This can be explained by observing the equivalent structure of the turbo encoder in Figure 3, where only systematic bits on the output of the RSC outer encoder is permuted by the deinterleaver and is then encoded by the inner encoder.

Upper bounds on the error rate achievable by maximum likelihood decoding of a turbo code have been obtained by a union bounding technique [4]. These bounds are expressed in terms of the joint input and output weight distribution of the constituent codes, with an assumption of random, independently chosen permutations of the input data before each constituent encoding. Two characteristic features of turbo code performance are the small Bit Error Rate (BER) achieved even at very low Signal-to-Noise Ratio (SNR) E_b/N_0 and the flattening of the error-rate curve – the so called "error floor" – at moderate and high values of SNR. An explanation for both of these phenomena was given by an analysis of the distance spectrum of turbo codes. It was shown in [5] that, at moderate-to-high SNR, the performance approaches the free-distance asymptote (theoretical bound) given by

$$P_{\text{free}} \approx \frac{N_{\text{free}}\overline{w}_{\text{free}}}{N} Q\left(\sqrt{d_{\text{free}}\frac{2RE_b}{N_0}}\right), \qquad (1)$$

where R is the code rate, d_{free} is the code free dis-

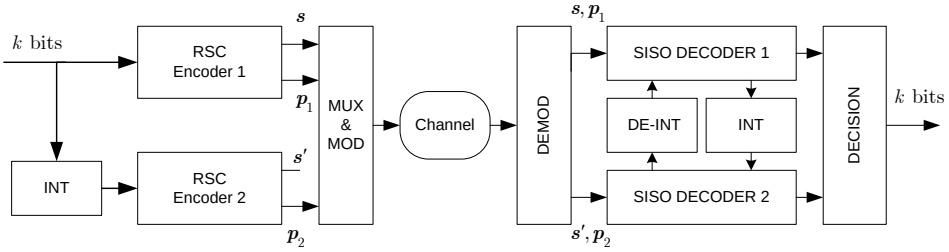

Figure 1. Structure of turbo encoder and decoder.

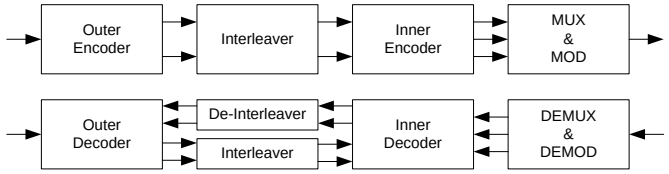

Figure 2. Structure for encoder and decoder of serially concatenated convolutional codes.

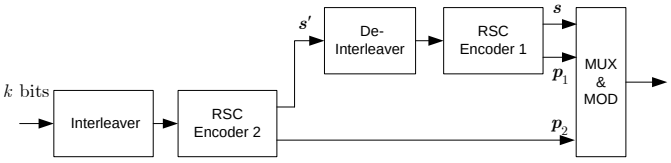

Figure 3. Equivalent serial concatenation structure of the turbo encoder.

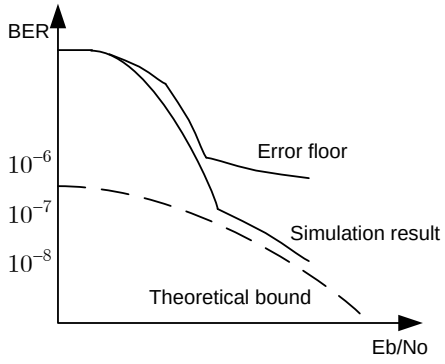

Figure 4. Illustration of turbo code error floor.

tance, N_{free} is the multiplicity of the minimum-weight codewords, N is the interleaver length, and $\overline{w}_{\text{free}}$ is the average information weight of input sequences causing free-distance codewords. The typical behavior of the BER curve of turbo encoders is shown in Figure 4.

The error floor of turbo codes is not an absolute lower limit on achievable error rate, but it is a region where the slope of the error rate curve becomes dramatically lower. This was basically due to poor interleaver design and/or truncations in the decoding algorithm. Many studies done in the last few years have shown that properly designed Parallel and Serial concatenated schemes have very low error floor, that they can perform at 0.1 dB from capacity (see [6] and references therein). Other theoretical and simulation results have shown that an accurate estimation of the SNR is not necessary [7], the decoder complexity is well within the capability of the current technology [8]–[10], and the delay is not at all significant at data rates used currently in almost all communication systems [11]. With a double-binary circular recursive systematic convolutional component code [12] used in a turbo scheme adopted for the DVB standard, no error floor appears regardless of the block size or coding rate down to BER of 10^{-8}. The same behavior was reported in [13] for serial concatenated codes and target BER of 10^{-10}.

For Gaussian channels, turbo coded modulation techniques can be broadly classified into binary schemes and Turbo Trellis Coded Modulation (TTCM) [14]. Bit interleaved coded modulation with iterative decoding (BICM-ID) [15] is a special case of serial concatenated codes where the encoder employs a convolutional code serially connected to a signal mapper through a bit interleaver. In the concept of TTCM, many studies have recently been done in the efforts to design BICM-ID systems in which a turbo code is employed at the transmitter to improve the spectral efficiency of the transmission using turbo codes [16]. In this paper, we show that the principle of BICM-ID can be extended to binary modulation schemes of turbo codes in order to improve their performance in the error floor region. If we consider the binary (± 1) modulated output 3-tuples of a rate-1/3 turbo encoder at each input bits as a 3-dimensional (3D) signal point, then a suitable mapping from 3-bit blocks in the output of the turbo encoder to the 8-point 3D signal cube creates three equivalent parallel binary channels with higher effective SNRs and, hence, gives raise to larger effective free distances. According to (1), this lowers the value of BER at the error floor.

The rest of the paper is organized as follows. In Section 2 we describe the system model for the new proposal for PCCC schemes. Section 3 is devoted to new SCCC schemes. Finally, some conclusions are presented.

2 Parallel Concatenation System Model for Modified Turbo Codes

Consider a structure of a generic turbo encoder consisting of two rate-1/2 recursive systematic convolutional (RSC) consistent encoders, concatenated in par-

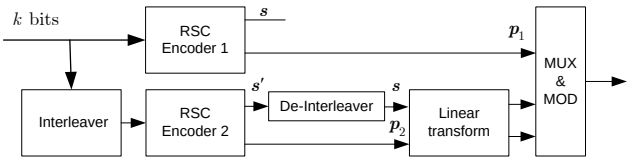

Figure 5. Parallel concatenation of a RSC code and a BICM subsystem.

allel through an interleaver π. Each data frame $\mathbf{u} = (u_1, u_2, \ldots, u_N)$ appears to the output of the turbo encoder as a sequence of information (systematic) bits $\boldsymbol{s} = (s_1, s_2, \ldots, s_N)$, where $s_n = u_n$, for $1 \leq n \leq N$, and at the same time is encoded by the first RSC encoder to form the parity check sequence $\mathbf{p}_1 = (p_{11}, p_{12}, \ldots, p_{1N})$. The interleaved version $\pi(\mathbf{u}) = (u_{\pi(1)}, u_{\pi(2)}, \ldots, u_{\pi(N)})$ of the information sequence $\mathbf{u}$ is encoded by the second RSC encoder to form the parity check sequence $\mathbf{p}_2 = (p_{21}, p_{22}, \ldots, p_{2N})$. Then $\mathbf{s}, \mathbf{p}_1$ and $\mathbf{p}_2$ are multiplexed and punctured if it is needed for coding rates higher than 1/3. Here we do not consider puncturing, so that we can denote the output of the turbo encoder by a sequence $\mathbf{c} = (\mathbf{c}_1, \mathbf{c}_2, \ldots, \mathbf{c}_N)$ of binary triplets $\mathbf{c}_n = (s_n, p_{1n}, p_{2n})$. From now on the index n and the index i satisfy $1 \leq n \leq N$ and $1 \leq i \leq 3$.

Consider the Additive White Gaussian Noise (AWGN) channel with Binary Phase Shift Keying (BPSK) modulation and one-side noise power spectral density N_0. Let the received signal sequence $\mathbf{r} = (\mathbf{r}_1, \mathbf{r}_2, \ldots, \mathbf{r}_N)$ consists of triplets

$$\mathbf{r}_n = (r_{n1}, r_{n2}, r_{n3}) = (s'_n, p'_{1n}, p'_{2n}) + (z_{n1}, z_{n2}, z_{n3}), \quad (2)$$

where z_{ni} are i.i.d. Gaussian noises with a zero mean and variance $\sigma^2 = N_0/2$, and triplets $\mathbf{s}_n = (s'_n, p'_{1n}, p'_{2n})$ are modulation signals corresponding to binary triplets $\mathbf{c}_n = (s_n, p_{1n}, p_{2n})$ under a mapping rule $\mathbf{c}_n = \mu(\mathbf{s}_n)$. Classic binary schemes of turbo codes have used bit-by-bit mapping from a bit $x \in \{0, 1\}$ onto a signal set $y \in \{\pm 1\}$ by the rule $y = 2x - 1$.

This paper proposes the removal of independence of the bit-by-bit mapping. Instead, we present a method of mapping each binary triplet into a set of 8 vertices of a 3D cube formed by modulated signal triplets, in such a manner that the combination of the turbo encoder and the modulator can be seen as a parallel concatenation of a RSC code and a BICM subsystem with an inline interleaver (Figure 5). In this figure, the combination of the second RSC encoder, the de-interleaver, and the modulator forms the BICM subsystem. Sequences $\mathbf{s}$ and $\mathbf{p}_1$ are correlated due to the structure induced by the first RSC encoder, while the sequence $\mathbf{p}_2$ is not correlated to the both of sequences $\mathbf{s}$ and $\mathbf{p}_1$ due to the interleaver. Thus the 3D mapping rules $\mathbf{c}_n = \mu(\mathbf{s}_n)$ can be reduced to a 2D mapping of pairs (s_n, p_{2n}), plus the traditional mapping rule for the bits p_{1n}. The iterative decoding in the receiver end can then exploit the advantage of different signal mapping in order to improve the system performance. Figure 6 shows some labelings of the 2D signals that are investigated in this paper. To employ the traditional bit-by-bit mapping in the block MUX∝MOD, pairs of bits (s_n, p_{2n}) are put through a linear transform which can be represented in the form of a matrix (2). Namely, with multiplication and addition operations in GF(2) we can write $(s_n^+, p_{2n}^+) = (s_n, p_{2n}) \times T$, where $T = G$ for Gray mapping, $T = A$ for the Mapping A, and $T = B$ for the Mapping B (see Figure 6). We note that Figure 5 is just to show the idea of using the BICM-ID principle for turbo codes. The linear transform, indeed, is performed directly on the sequences $\mathbf{s}$ and $\mathbf{p}_2$ on the output of the turbo encoder.

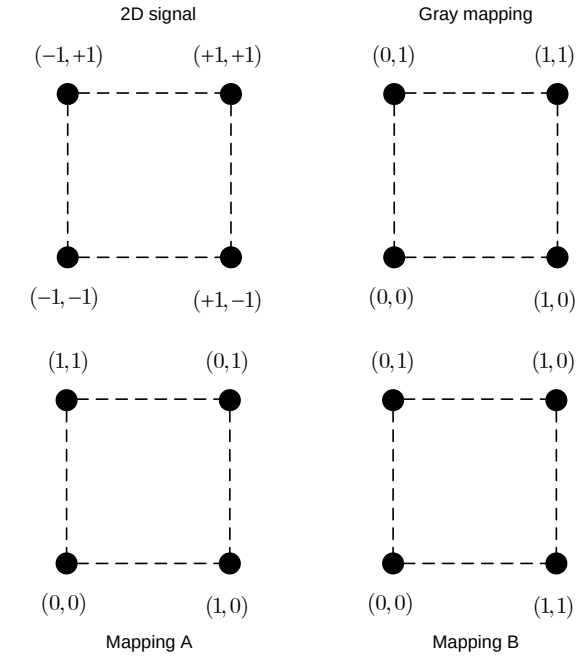

Figure 6. Different mappings of the 2D signals.

$$G = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} A = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} B = \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix} \quad (3)$$

Accordingly, the decoder now performs an iterative decoding that exchanges extrinsic information between a Soft-Input Soft-Output (SISO) decoder for the corresponding BICM-ID system [15] and a SISO decoder for the RSC code. The SISO decoder for the BICM-ID subsystem is formed by a SISO decoder for the RSC code and a Symbol-to-Bit Converter (SBC), which computes Log-Likelihood Ratios (LLRs) of the coded bits based on the received signals. In this paper we employ the A Posteriori Probability (APP) decoder [17] to decode RSC codes. The SBC is designed as follows.

Each channel observation triplet $\mathbf{r}_n = (r_{n1}, r_{n2}, r_{n3})$ is fed to the BSC together with the a priori information $L_A(c_{ni})$ as a feedback from the update channel information L'_c of the first and second SISO decoders (at the first iteration these values are set to zero). The Log-Likelihood ratio values $\mathrm{LLR}(c_{ni}|\mathbf{r}_n)$ of bits c_{ni}, for

$1 \le n \le N$ and $1 \le i \le 3$, are computed as follows [18]:

$$\mathrm{LLR}(\mathbf{c}_{ni}|\mathbf{r}_n) = L_A(c_{ni}) + \ln \frac{\sum_{s_n \in S_{i,1}} P(\mathbf{r}_n|\mathbf{s}_n) \exp(\frac{1}{2}\langle \mathbf{c}_{n,[i]}, L_{A,[i]} \rangle)}{\sum_{\mathbf{s}_n \in S_{i,0}} P(\mathbf{r}_n|\mathbf{s}_n) \exp(\frac{1}{2}\langle \mathbf{c}_{n,[i]}, L_{A,[i]} \rangle)}, \quad (4)$$

where $S_{i,u} = \{\mathbf{s}_n = \mu(\mathbf{c}_n) : c_{ni} = u\}$ is defined as a subset consisting of signals whose binary label has the bit $u \in \{0,1\}$ in the i-th position according to the mapping rule μ. Denote by $\langle \boldsymbol{a}, \boldsymbol{b} \rangle$ the inner product of two vectors. Let $\mathbf{c}_{n,[i]}$ be a vector resulted from $\mathbf{c}_n$ by deleting its i-th component, and let $L_{A,[i]}$ be a vector resulted from L_A by deleting its i-th component. For the AWGN channel we have [18]

$$P(\mathbf{r}_n|\mathbf{s}_n) = \frac{\exp(-\frac{1}{2\sigma^2} \parallel \mathbf{r}_n - \mathbf{s}_n \parallel^2)}{\sqrt{2\pi\sigma^2}}. \quad (5)$$

The sequence of values $\mathrm{LLR}(c_{n1})$ is permuted by the same interleaver as in the turbo encoder. The permuted sequence is then interlaced with the sequence $\mathrm{LLR}(c_{n3})$ to form a sequence of channel observation pairs $(\mathrm{LLR}(c_{n1}), \mathrm{LLR}(c_{n3}))$ which are fed to the input L_c of the second SISO decoder. Input L_u of the second SISO decoder is the permuted sequence of the updated extrinsic information L'_u of the first decoder (at the first iteration these values are set to zero). The sequence of updated extrinsic information on the output L'_u of the second decoder is de-interleaved and is then fed back to the first decoder together with channel observations $\mathrm{LLR}(c_{n2})$.

We present simulation results for modified turbo codes (PCCC) in Figures 7, 8, 9 and 10. For constituent 4-state RSC encoder of generators $[1 + D + D^2, 1 + D^2]$ (with $1 + D + D^2$ as the feedback), simulation is done for interleaver lengths of 512, 2048, and 4096 bits. For the component 8-state RSC encoder we give simulation results for the 512-bit interleaver. To ease the interleaver generation, we use the algorithm which has been proposed for WCDMA. It can be seen in figures that both of Mapping A and Mapping B has significantly improved the performance of the PCCC scheme in the error floor region.

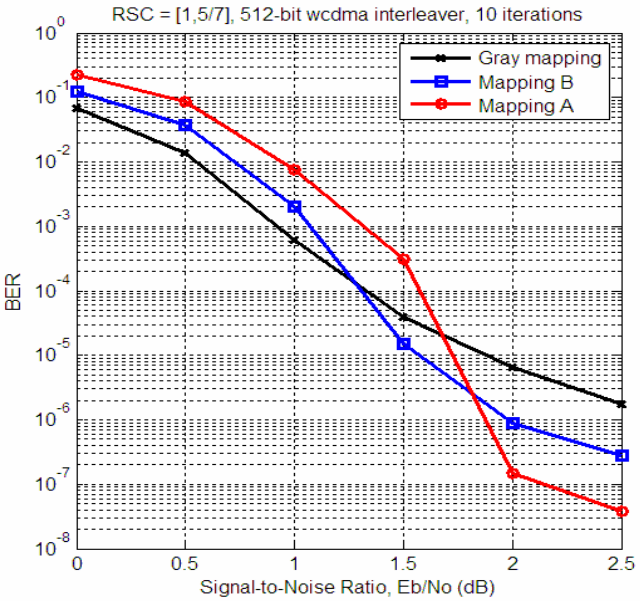

Figure 7. Comparison of modified 4-state PCCC with different mappings and a 512-bit interleaver.

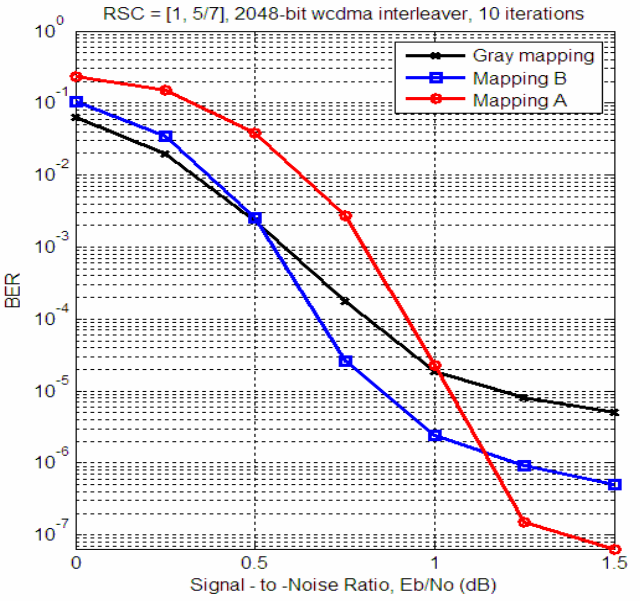

Figure 8. Comparison of modified 4-state PCCC with different mappings and a 2048-bit interleaver.

3 Serial Concatenation System Model

Consider the serial concatenation of convolutional codes as depicted in Figure 2, where the outer code is a rate $-1/2$ RSC code and the inner code is a rate $-2/3$ RSC code, so that the overall coding rate is equal to $1/3$. Each data frame $\mathbf{u} = (u_1, u_2, \ldots, u_N)$ appears to the output of the outer encoder as a sequence of information (systematic) bits $\mathbf{s} = (s_1, s_2, \ldots, s_N)$, where $s_n = u_n$, for $1 \le n \le N$, and at the same time is encoded by the outer encoder to form the parity check sequence $\mathbf{p}_1 = (p_{11}, p_{12}, \ldots, p_{1N})$. The interlaced sequence $(\mathbf{s}, \mathbf{p}_1) = (s_1, p_{11}, s_2, p_{12}, \ldots, s_N, p_{1N})$ is permuted by the interleaver π which now has a length of $2N$ bits. In the original SCCC scheme, the interleaved version is encoded by the inner encoder to form the parity check sequence $\mathbf{p}_2 = (p_{21}, p_{22}, \ldots, p_{2N})$. Then $\mathbf{s}, \mathbf{p}_1$ and $\mathbf{p}_2$ are multiplexed so that we can denote the output of the SCCC encoder by a sequence $\mathbf{c} = (\mathbf{c}_1, \mathbf{c}_2, \ldots, \mathbf{c_N})$ of binary triplets $\mathbf{c}_n = (s_1, p_{1n}, \ldots, p_{2n})$. We consider the binary (± 1) modulated output 3-tuples as a 3-dimensional (3D) signal point, then the combination of the best rate $-2/3$ RSC encoder in the term of a largest Hamming free distance and the Gray mapping of its outputs to the 3D signal points obviously gives rise to a best trellis-coded modulation (TCM) code, namely, in the term of a largest free squared Euclidean distance.

Let us observe the equivalent representation of turbo encoder structure as a serial concatenation of RSC codes in Figure 2. In this configuration the RSC ENCODER2

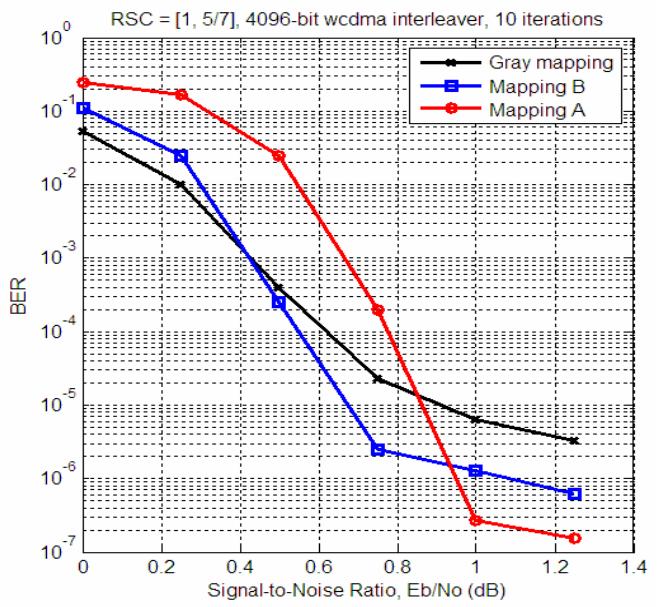

Figure 9. Comparison of modified 4-state PCCC with different mappings and a 4096-bit interleaver.

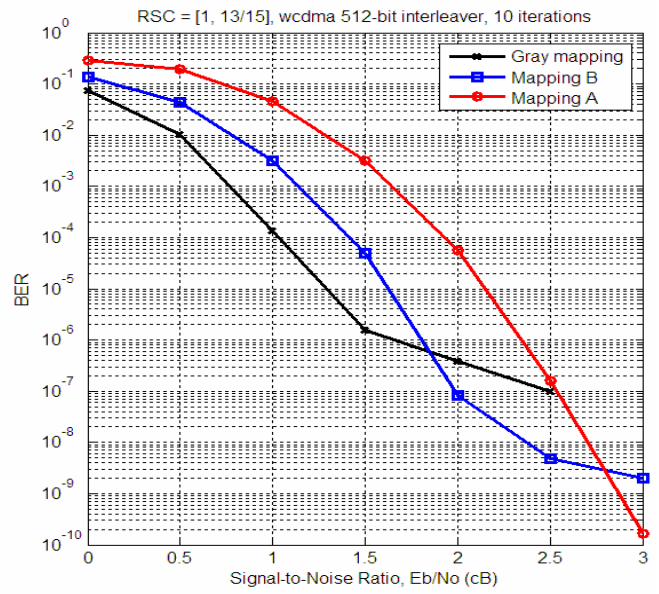

Figure 10. Comparison of modified 8-state PCCC with different mappings and a 512-bit interleaver.

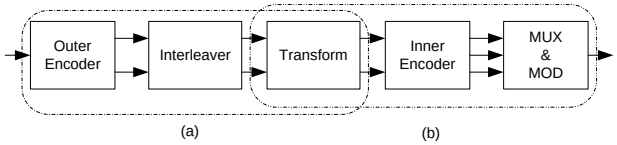

Figure 11. Serial concatenation of a RSC code and a coded modulation subsystem.

plays a role of the outer encoder, while the RSC ENCODER1 is the inner encoder. Then the BICM principle applied to the parallel concatenation system can be extended to the serial concatenation system as it is depicted in Figure 11. The linear transform $T = G$, A, or B is applied to the permuted version of the sequence $(\mathbf{s}, \mathbf{p}_1) = (s_1, p_{11}, s_2, p_{12}, \ldots, s_N, p_{1N})$ before

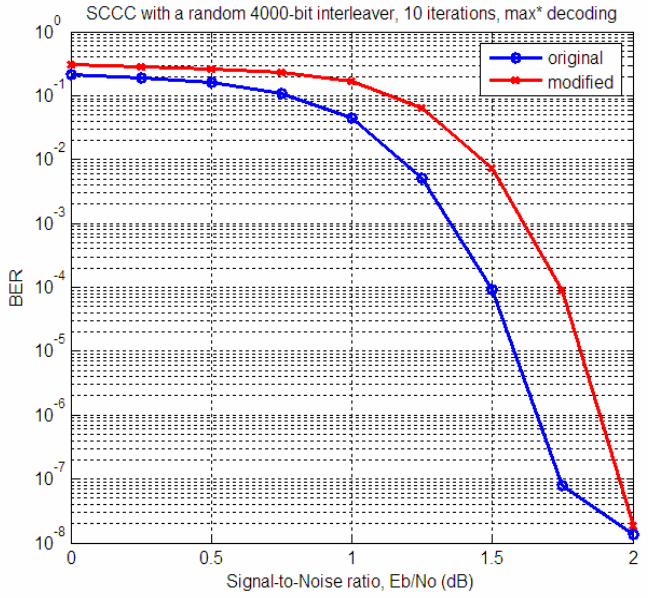

Figure 12. Comparison of the original SCCC and the modified SCCC.

the permuted sequence is fed to the inner encoder. Part a) in Figure 11 forms a BICM system. We note that the linear transform can be combined with the inner encoder, which is also a linear transform, to form a new encoder for the inner code. The trellis representation of the new inner encoder can be obtained from the trellis representation of the original inner encoder by swapping two input bit pairs according to the applied transform. Namely, for $T = G$ there is no need for any modification of the innerencoder. For $T = A$, the trellis transitions according to input pairs '01' and '11' are swapped. For $T = B$, the trellis transitions according to input pairs '10' and '11' are swapped. In the same manner we can obtain the labeling of vertices of squares for the mapping A and the mapping B in Figure 6 from the labeling of the square representing Gray mapping.

The decoding is now even simpler than the decoding in the parallel concatenation system, since there is no need for the symbol-to-bit converter. The trellis for the APP decoder of the inner code is modified in the same manner as it has been done in the encoder. Beside this small modification, all decoding processes are the same as in decoding of SCCC schemes. Note that if $T = G$, i. e., when Gray mapping is used, there is not any modification and, hence, both of the parallel and serial concatenation systems turn out to be the original PCCC and SCCC schemes, respectively.

Figure 12 shows the simulation results for the original SCCC with a 4000-bit random interleaver. The 8-state rate $-1/2$ outer RSC has the generators $[1 + D + D^2, 1 + D^2]$ (with $[1 + D + D^2]$ as the feedback). The 16-state rate $-2/3$ inner RSC has the generators

$$\begin{bmatrix} 1 + D + D^2 & 0.1 + D^2 \\ 0.1 + D + D^2 & 1 + D \end{bmatrix}, \tag{6}$$

with $1 + D + D^2$ as the feedbacks. We suppose that the modified SCCC will show a lower error floor than the original SCCC does. There is no difference in the

performance of the modified SCCC with mapping A or B, since the interleaver is assumed to be an overall interleaver. Remember that the interleaver in the modified PCCC scheme is the inline interleaver.

4 Conclusion

We have presented a way of lowering the error floor of PCCC as well as SCCC with BPSK modulation and the AWGN channel. The new idea is to consider, in general, the binary modulation of triplets of the PCCC and SCCC output bits as 3D mappings, so that the PCCC and the SCCC schemes can be transformed into parallel and serial concatenation, respectively, of a BICM system and a binary convolutional code. These schemes are not the known TTCM schemes, since they deal with binary modulation and, hence, are much simpler. The simulation results have shown that new PCCC and SCCC codes perform better than the original codes in the error floor region. More importantly, this is done with only a small modification in the encoders and decoders.

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